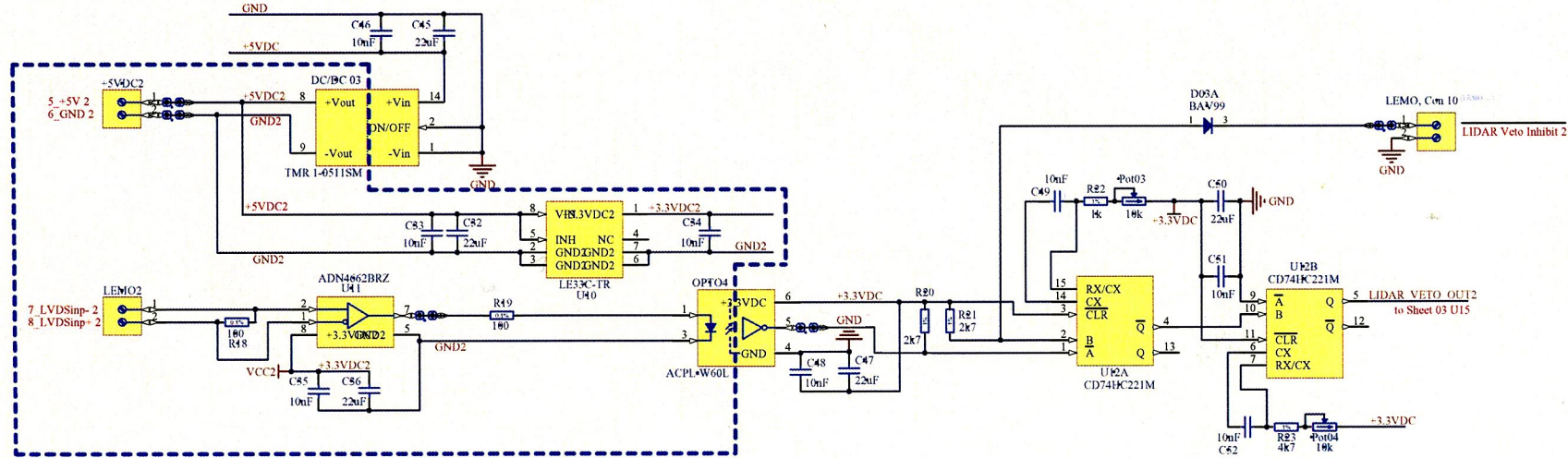
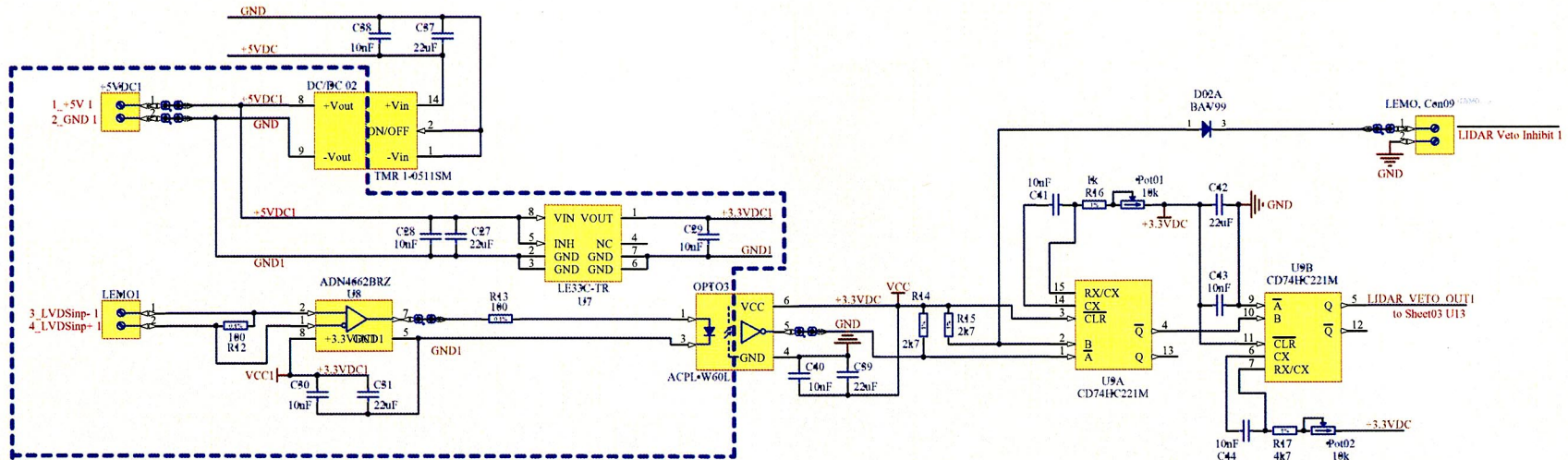
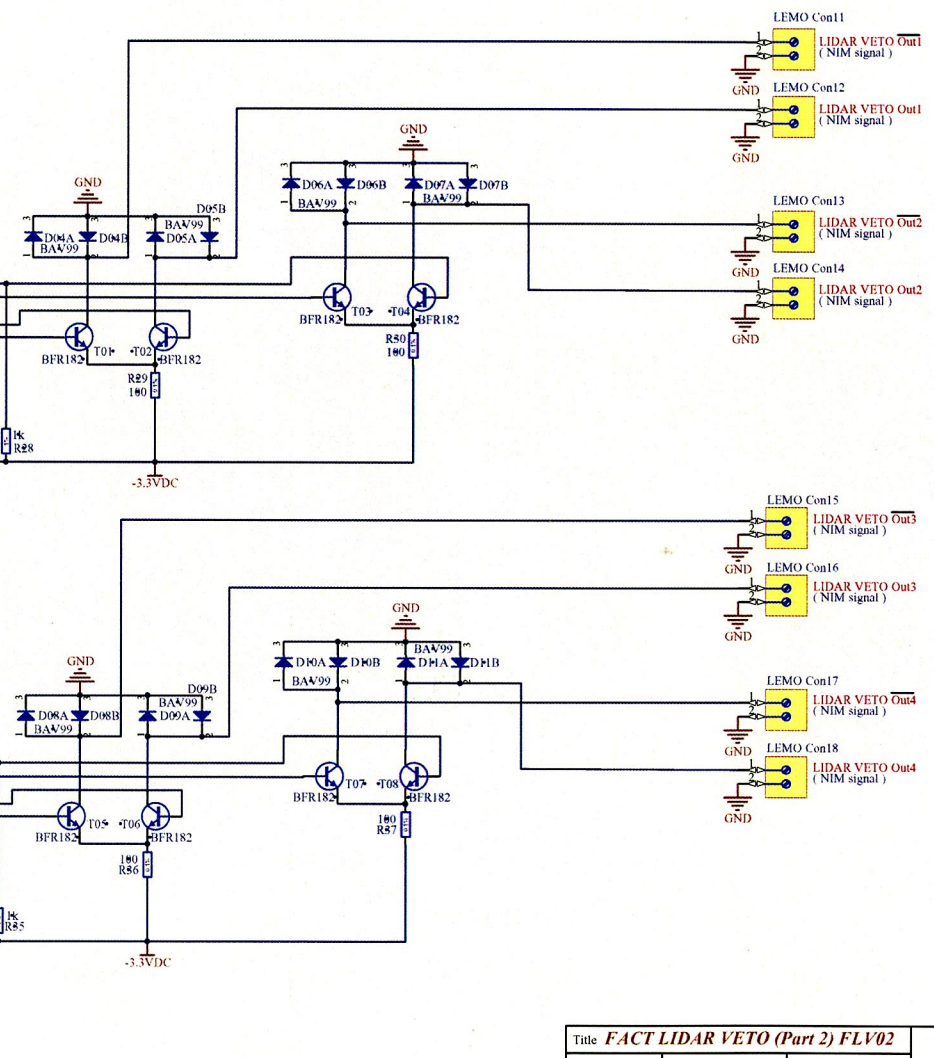
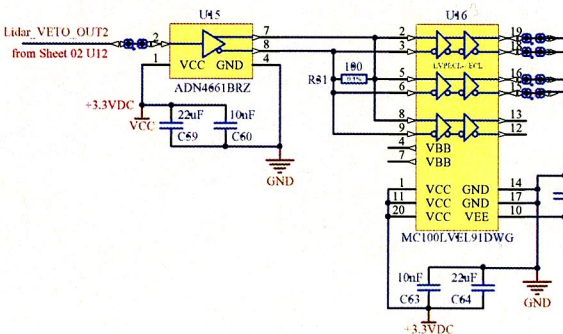
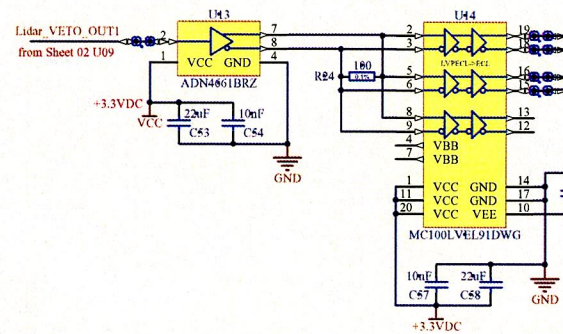
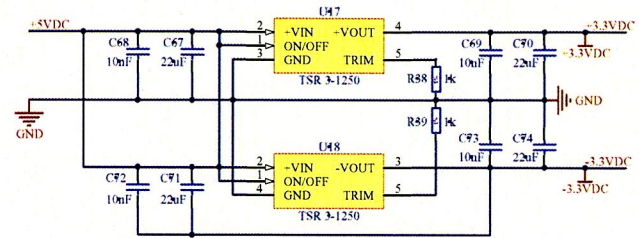
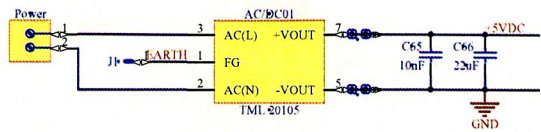
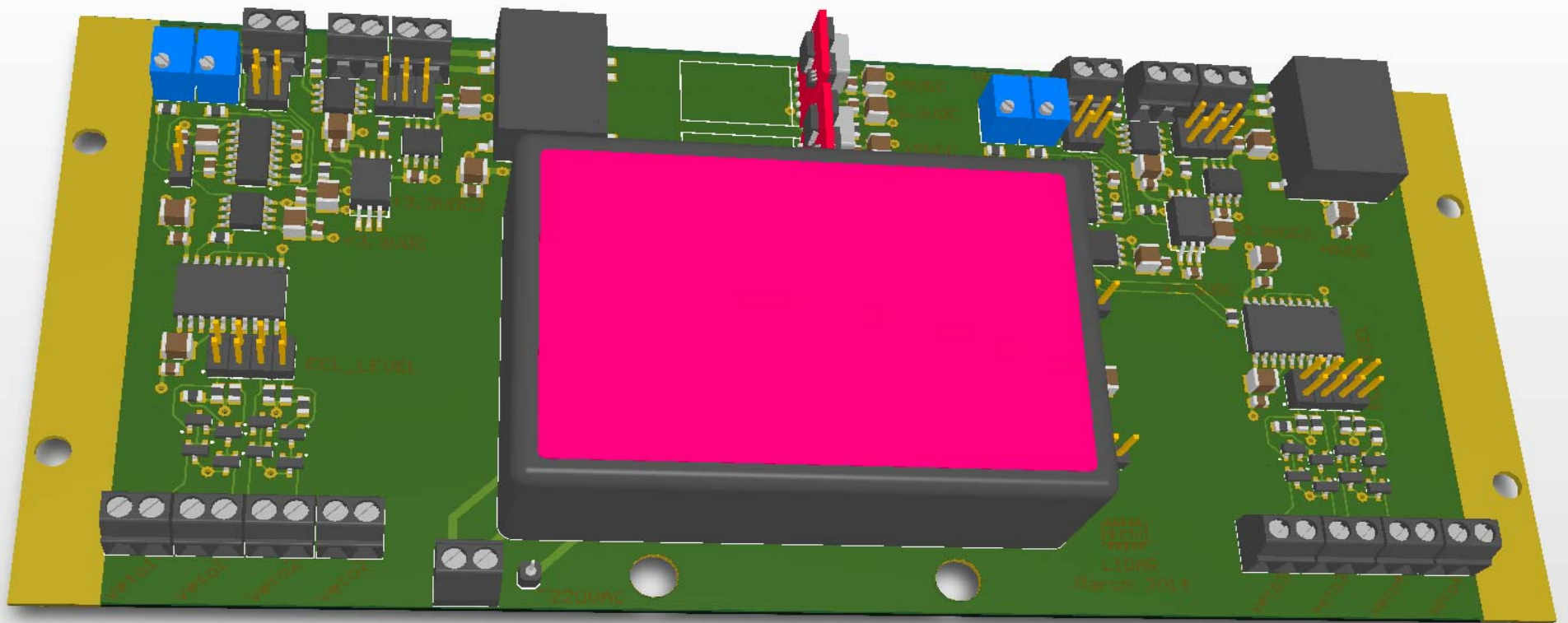


LIDAR1  
LIDAR1.SCHDOC





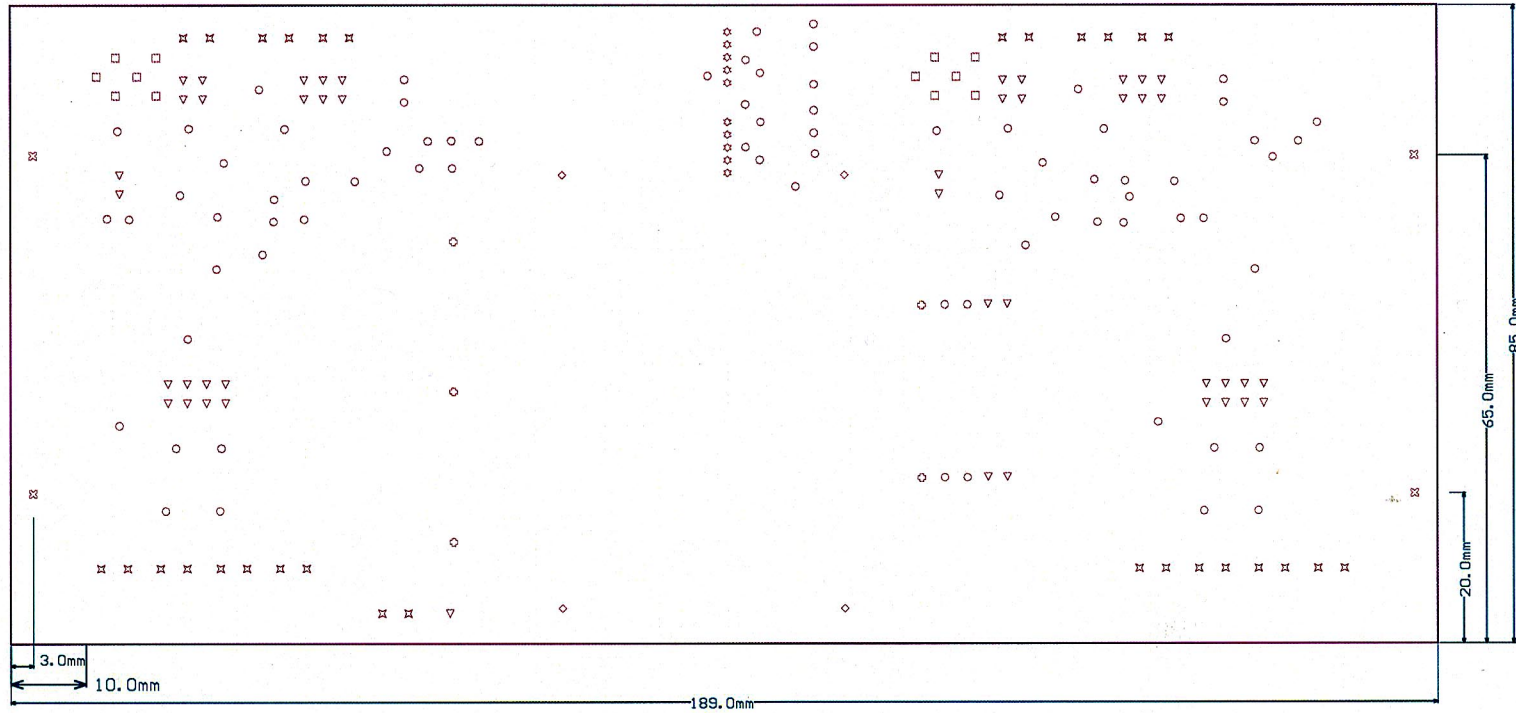




# FACT LIDAR Veto (Part 2 (FACT Side))

board dimension & drill drawing

page 01 of 10



IPP / ETHZ

LD / HPvG

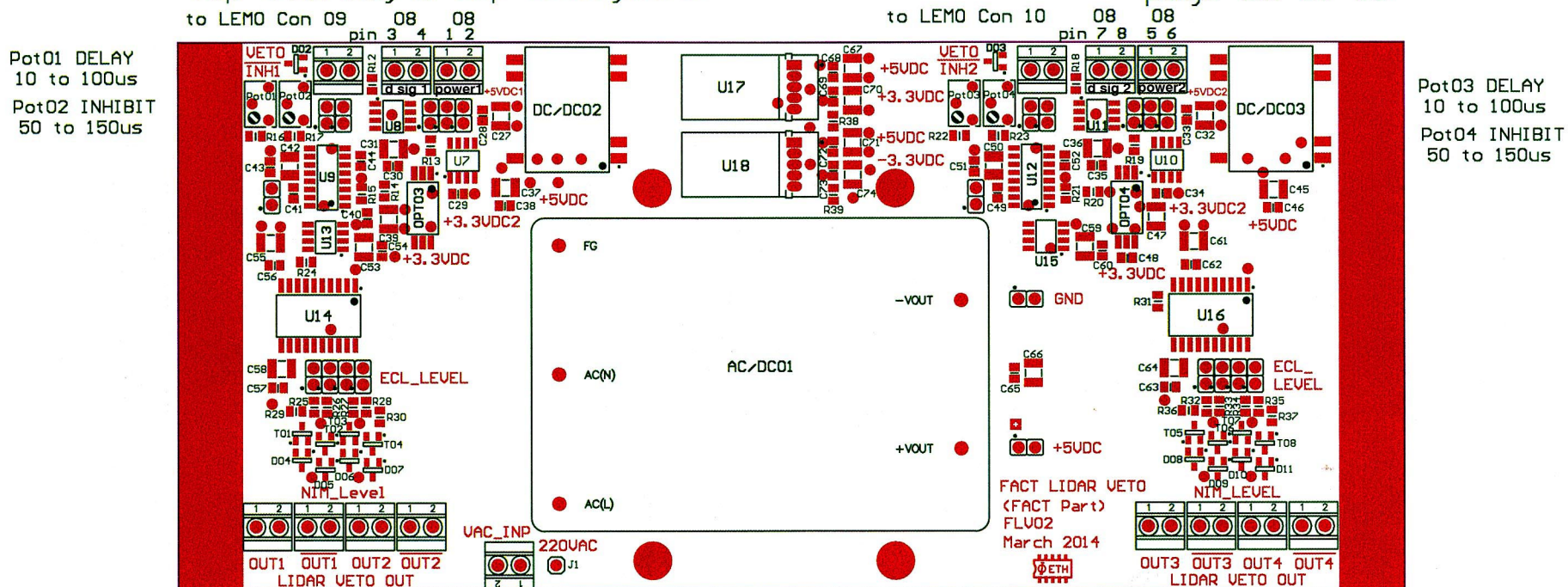
M:1:1

April 2014

# FACT LIDAR Veto (Part 2 (FACT Side))

top overlay & top designator

page 02 of 10



Pot01 DELAY  
10 to 100us  
Pot02 INHIBIT  
50 to 150us

Pot03 DELAY  
10 to 100us  
Pot04 INHIBIT  
50 to 150us

to LEMO Con 11 12 13 14 to AC Inp  
Filter & Switch

to LEMO Con 15 16 17 18

IPP / ETHZ

LD / HPvG

M:1:1

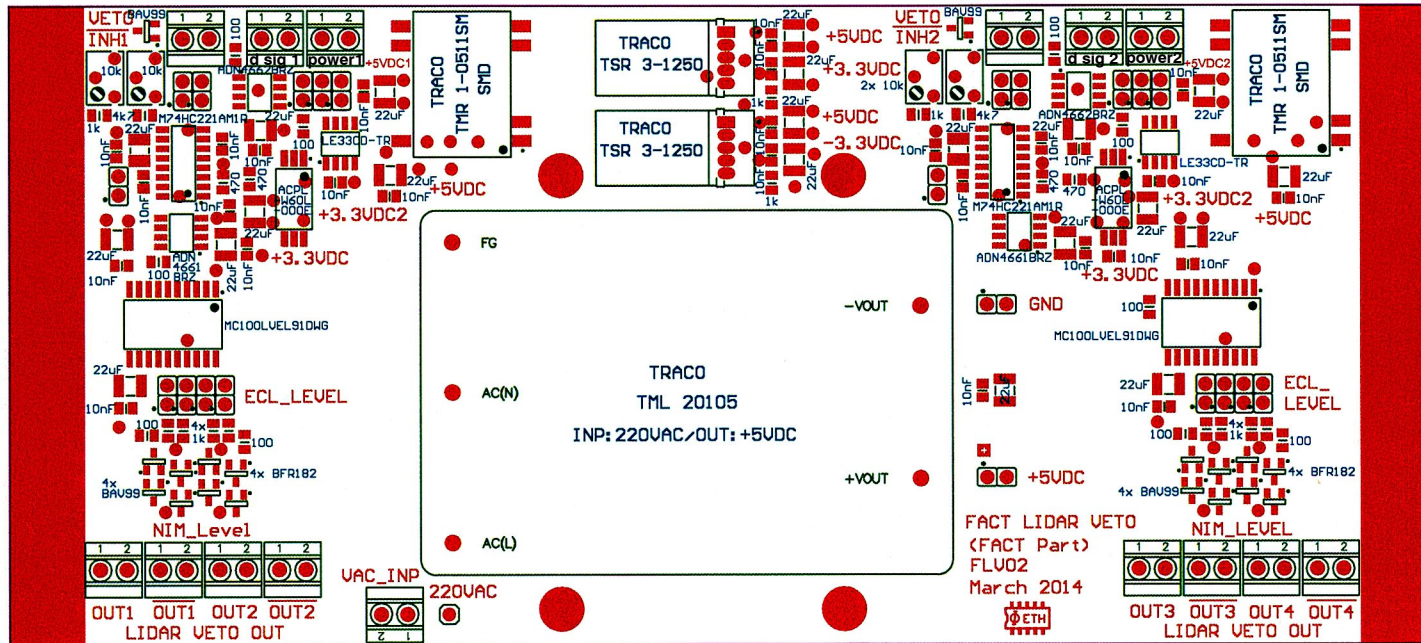
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# FACT LIDAR Veto (Part 2 (FACT Side))

top overlay & top comment

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- all resistor size 0805
- all 10nF capacitor size 0805
- all 22uF capacitor size 1210
- all diode BAU99 size SOT23
- all transistor BFR182 size SOT23
- LE33CD-TR size 8SO
- ADN4661BRZ size 8SOIC
- ADN4662BRZ size 8SOIC
- ACPL-W60L-000E size 6SO
- CD74HC221AM1R size 16SOIC
- MC100LVEL91D4G size 20SOIC

IPP / ETHZ

LD / HPvG

M:1:1

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# FACT LIDAR Veto (Part 2 (FACT Side))

top paste

page 04 of 10



IPP / ETHZ

LD / HPvG

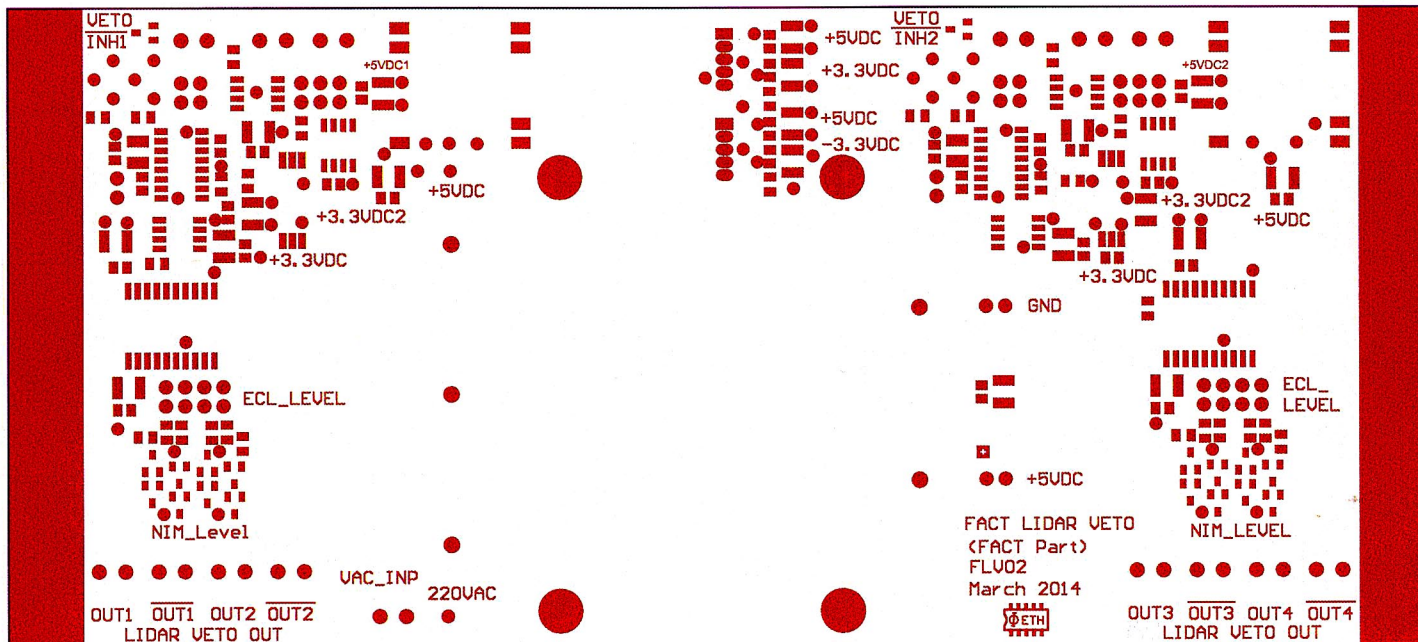
M:1:1

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# FACT LIDAR Veto (Part 2 (FACT Side))

top solder

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IPP / ETHZ

LD / HPvG

M:1:1

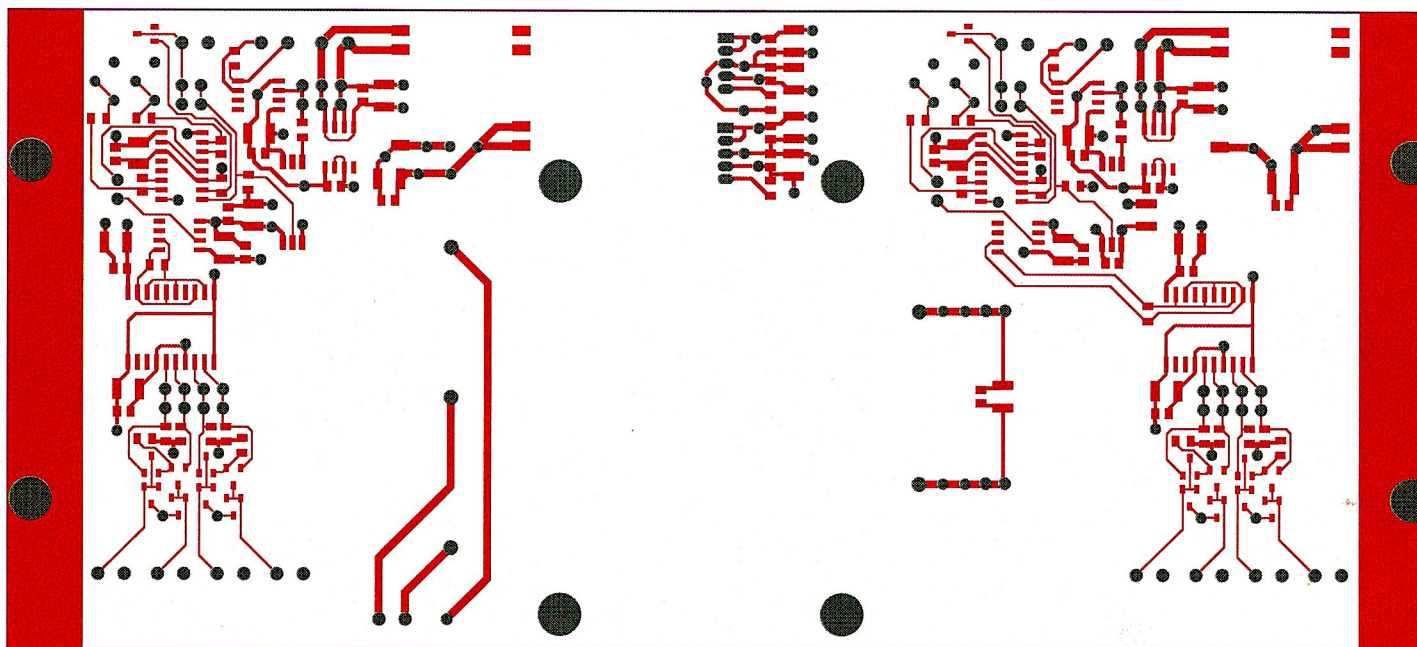
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# FACT LIDAR Veto (Part 2 (FACT Side))

top layer

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IPP / ETHZ

LD / HPvG

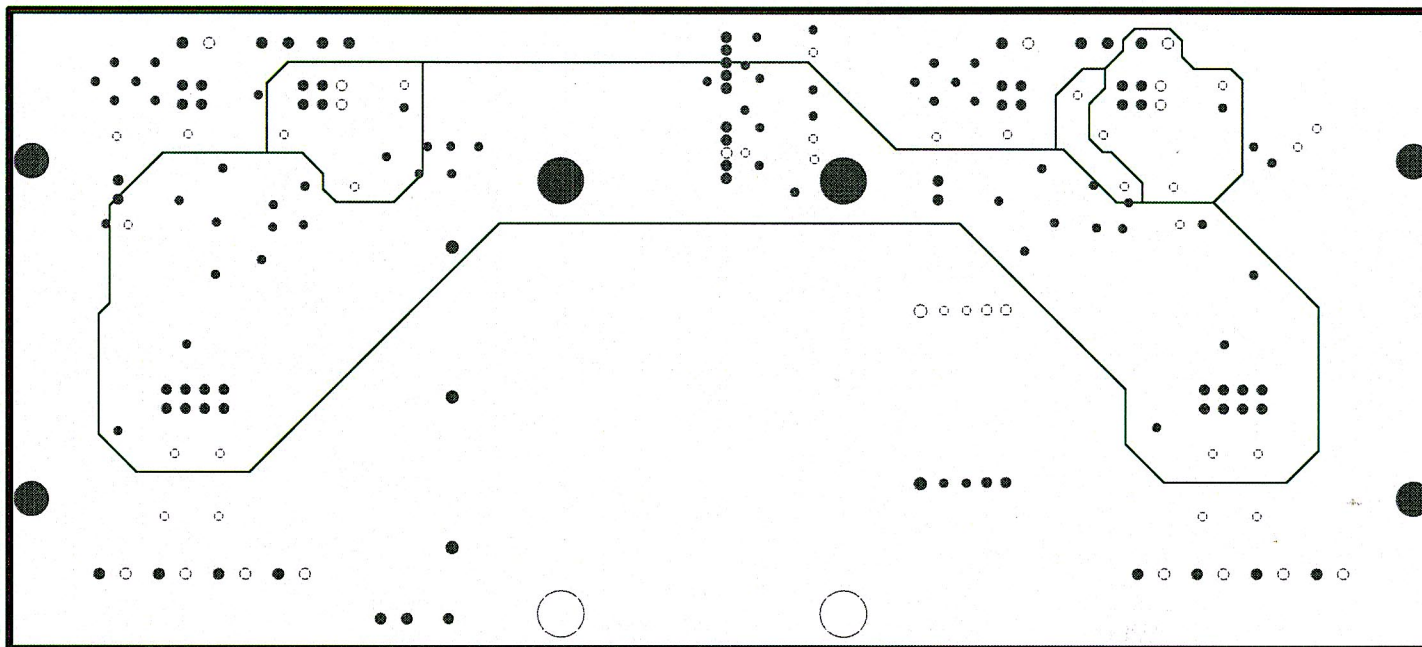
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# FACT LIDAR Veto (Part 2 (FACT Side))

plane 1 (GND)

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IPP / ETHZ

LD / HPvG

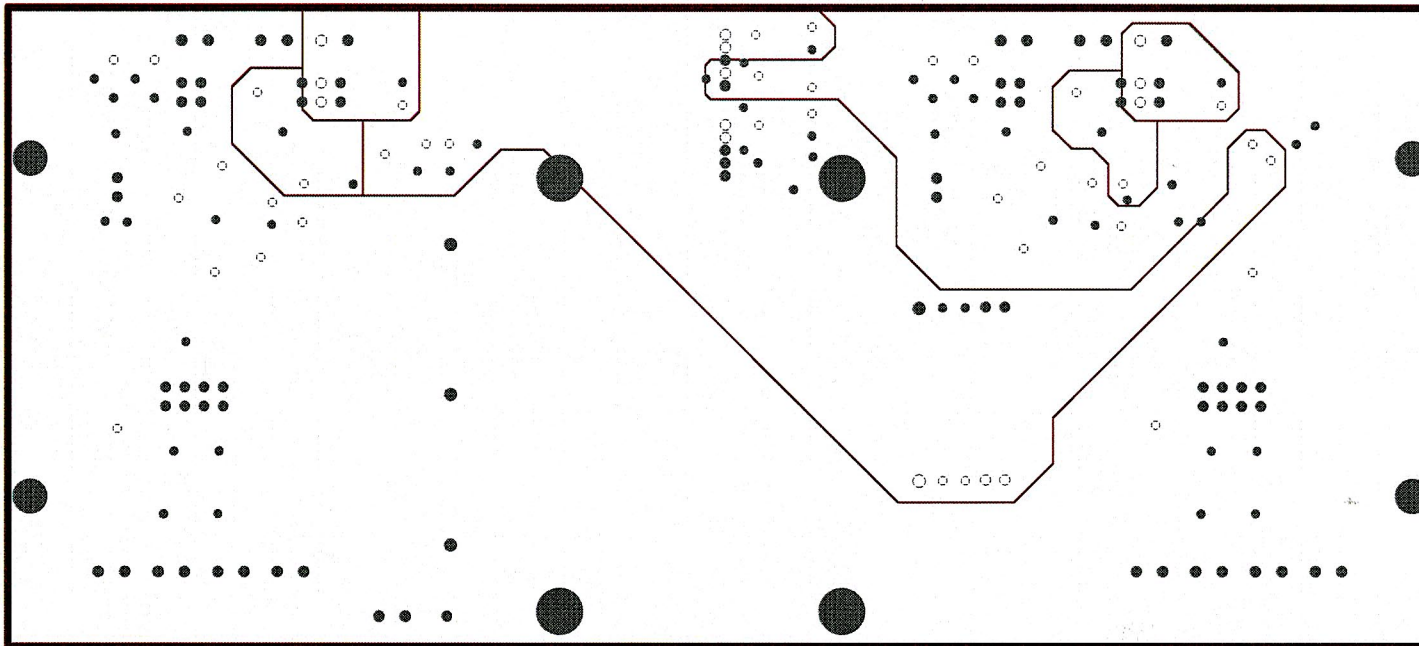
M:1:1

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# FACT LIDAR Veto (Part 2 (FACT Side))

plane 2 (power)

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IPP / ETHZ

LD / HPvG

M:1:1

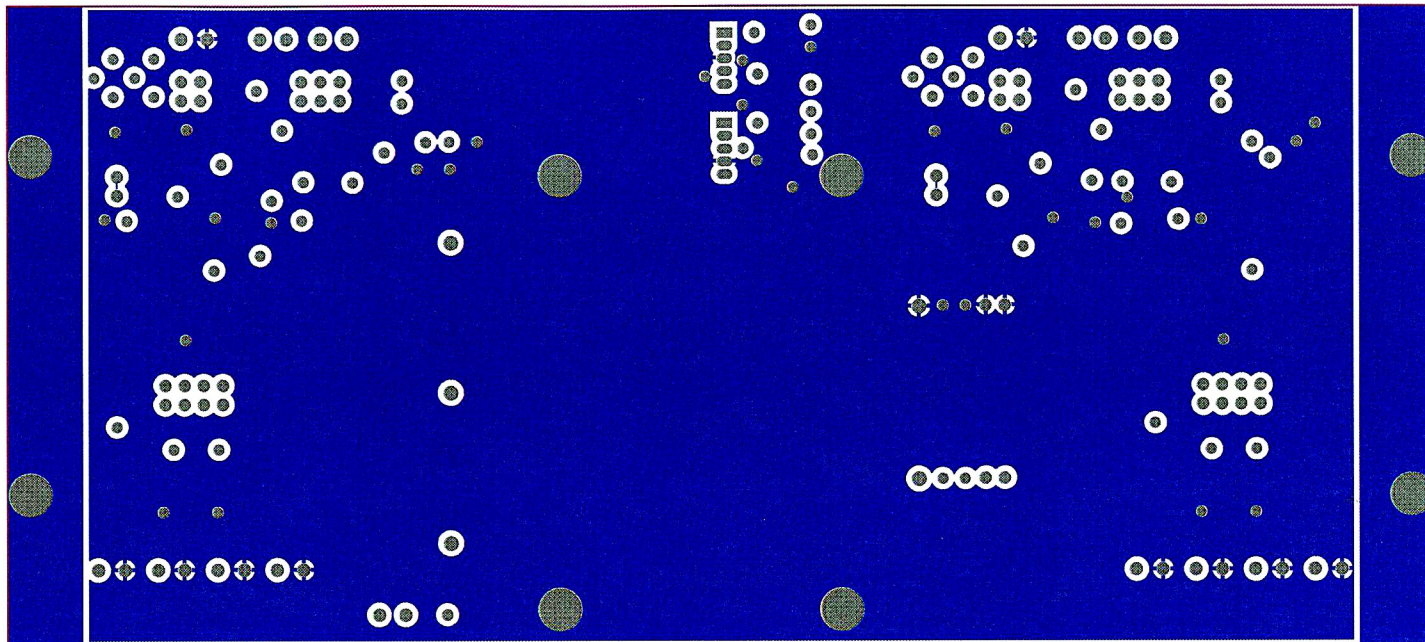
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# FACT LIDAR Veto (Part 2 (FACT Side))

bottom layer

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IPP / ETHZ

LD / HPvG

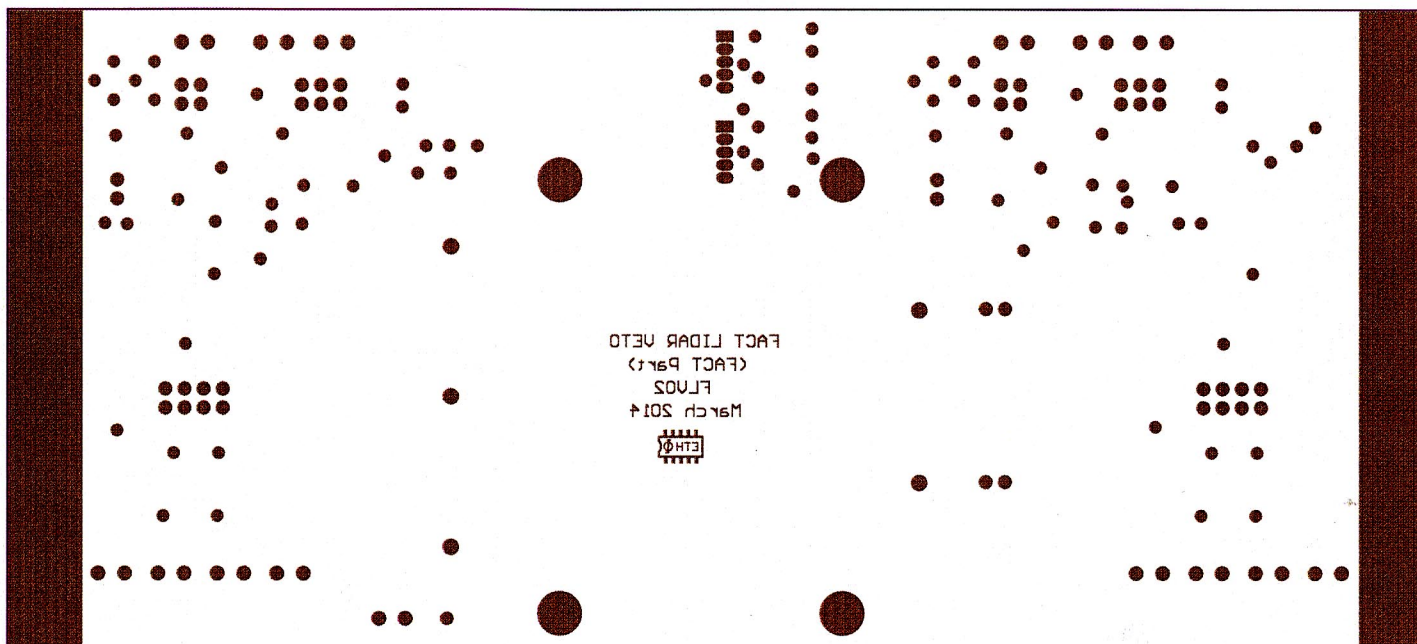
M:1:1

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# FACT LIDAR Veto (Part 2 (FACT Side))

bottom solder

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IPP / ETHZ

LD / HPvG

M:1:1

April 2014